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Substitute for form 1449/PTO NINTH SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/700,485
				Filing Date	November 5, 2003
				First Named Inventor	Le Trong NGUYEN
				Art Unit	2183
				Examiner Name	Daniel H. Pan
Sheet	1	of	1	Attorney Docket Number	1397.028000H (SP015.C17)

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	4,980,817	12-25-1990	Fossum et al.	
	US2	5,179,689	01-12-1993	Leach et al.	
	US3	5,249,286	09-28-1993	Alpert et al.	
	US4	5,590,295	12-31-1996	Deosaran et al.	
	US5	5,617,554	04-01-1997	Alpert et al.	
	US6	5,630,157	05-13-1997	Dwyer, III	
	US7	5,745,375	04-28-1998	Reinhardt et al.	
	US8	5,802,605	09-01-1998	Alpert et al.	
	US9	5,809,276	09-15-1998	Deosaran et al.	
	US10	5,819,101	10-06-1998	Peleg et al.	
	US11	5,826,055	10-20-1998	Wang et al.	
	US12	5,881,275	03-09-1999	Peleg et al.	
	US13	6,131,157	10-10-2000	Wang et al.	
	US14	6,138,231	10-24-2000	Deosaran et al.	
	US15	6,272,617	08-07-2001	Deosaran et al.	
	US16	6,385,634	05-07-2002	Peleg et al.	
	US17	6,418,529	07-09-2002	Roussel	
	US18				
	US19				
	US20				

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
	FP1					
	FP2					
	FP3					
	FP4					
	FP5					
	FP6					
	FP7					
	FP8					
	FP9					

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	<i>Complaint</i> , 7 pages, dated October 11, 2006, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL2	<i>First Amended Complaint</i> , 7 pages, dated December 12, 2006, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL3	<i>Intel Corporation's Answer, Affirmative Defenses, and Counterclaims to Transmeta's First Amended Complaint</i> , 27 pages, dated January 9, 2007, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL4	<i>Intel Corporation's Responses to Transmeta's First Set of Interrogatories to Intel Corporation (Nos. 1-24) - Redacted Public Version</i> , 132 pages, dated May 18, 2007, in Transmeta Corporation v. Intel Corporation, in the U.S. District for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL5	<i>Intel Corporation's Supplemental Responses to Transmeta Interrogatory Nos. 8, 9, 12, 19, and 21-23 - Redacted Public Version</i> , 27 pages, dated August 23, 2007, in Transmeta Corporation v. Intel Corporation, in the U.S. District for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL6	<i>Intel Corporation's Opening Claim Construction Brief</i> , 76 pages, dated October 19, 2007, in Transmeta Corporation v. Intel Corporation, in the U.S. District for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL7	<i>Transmeta Corporation's Opening Claim Construction Brief</i> , 66 pages, dated October 19, 2007, in Transmeta Corporation v. Intel Corporation, in the U.S. District for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL8	<i>Stipulation of Dismissal</i> , 1 page, dated January 31, 2008, in Transmeta Corporation v. Intel Corporation, in the U.S. District Court for the District of Delaware, Case No. 1:06-cv-00633.	
	NPL9	Order Granting Request for Ex Parte Reexamination, mailed May 11, 2007 in Control No. 90/008,569, 27 pages.	
	NPL10	Order Granting Request for Ex Parte Reexamination, mailed May 11, 2007 in Control No. 90/008,573, 17 pages.	

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL11	Order Granting Request for Ex Parte Reexamination, mailed June 12, 2007 in Control No. 90/008,585, 19 pages.	
	NPL12	Order Granting Request for Ex Parte Reexamination, mailed June 16, 2007 in Control No. 90/008,644, 35 pages.	
	NPL13	Order Granting Request for Ex Parte Reexamination, mailed August 13, 2007 in Control No. 90/008,691, 20 pages.	
	NPL14	Order Granting Request for Ex Parte Reexamination, mailed August 29, 2007 in Control No. 90/008,712, 16 pages.	
	NPL15	Adams et al., "Utilizing low level parallelism in general purpose code: the HARP project," Microprocessors and Microsystems, Vol. 29, No. 3 (Oct. 1990).	
	NPL16	Albert, AJ, "User Configurable Local Storage Registers," IBM Technical Disclosure Bulletin, pp. 3971-3975 (1976).	
	NPL17	Butler, M. and Patt, Y., "An Improved Area-Efficient Register Alias Table for Implementing HPS," University of Michigan, Ann Arbor, Michigan, 24 pages (January 1990).	
	NPL18	Butler, M. et al., "Single Instruction Stream Parallelism Is Greater than Two," Proceedings of the 18th Annual International Symposium on Computer Architecture, ACM, pp. 276-286 (May 1991).	
	NPL19	Colwell, R. et al., "Architecture and implementation of a VLIW supercomputer," Proc. Of the 1990 Conf. on Supercomputing (1990).	
	NPL20	Convex Architecture Handbook, Version 1, Convex Computer Corporation (1984).	

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL21	Fairchild Semiconductor "Clipper 32-Bit Microprocessor - User's Manual," Prentice-Hall, Inc. (1987).	
	NPL22	Huang, J.W. et al., "Dynamically Reconfigurable Vectors," IBM Technical Disclosure Bulletin, pp. 3480-3483 (Dec. 1980).	
	NPL23	Hwu, W. and Patt, Y., "Design Choices for the HPSm Microprocessor Chip," Proceedings of the Twentieth Annual Hawaii International Conference on System Sciences, pp. 330-336 (1987).	
	NPL24	Hwu, W. and Patt, Y., "HPSm2: A Refined Single-Chip Microengine," HICSS '88, IEEE, pp. 30-40 (1988).	
	NPL25	Hwu, W-M. et al., "An HPS Implementation of VAX: Initial Design and Analysis," Proceedings of the Nineteenth Annual Hawaii International Conference on System Sciences, pp. 282-291 (1986).	
	NPL26	Intrater et al., "A Superscalar Microprocessor," IEEE Proceedings of the 17th Convention of Electrical & Electronics Engineers In Israel, pp. 267-270 (March 1991).	
	NPL27	Maejima et al., "A 16-bit Microprocessor with Multi-Register Band Architecture," Proc. Fall Joint Computer Conference, pp. 1014-1019 (Nov. 2-6, 1986).	
	NPL28	Maly et al., Memory Chip for 24-Port Global Register File, Custom Integrated Circuits Conference, Proceedings of the IEEE, (published May 12, 1991).	
	NPL29	Margulis, N., "i860 microprocessor internal architecture," Microprocessors and Microsystems, Butterworth & Co. Ltd., Vol. 14, No. 2, pp. 89-96 (March 1990).	
	NPL30	Melear, "The Design of the 88000 RISC Family," IEEE Micro, Vol. 9, No.2, pp. 26-38 (April 1989).	

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Sheet	4	of	4		

NON PATENT LITERATURE DOCUMENTS

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	NPL31	Myers et al., The 80960 Microprocessor Architecture, John Wiley & Sons, Inc (1988).	
	NPL32	Paper No. 28 (Office Action dated June 19, 1996) from U.S. Application No. 08/481,146.	
	NPL33	Paper No. 32 (Office Action dated November 18, 1996) from U.S. Application No. 08/481,146.	
	NPL34	Patt et al., "Run-Time Generation of HPS Microinstructions From a VAX Instruction Stream," Proceedings of MICRO 19 Workshop, New York, pp. 75-81 (October 1986).	
	NPL35	Patt, Y.N. et al., "Experiments with HPS, a Restricted Data Flow Microarchitecture for High Performance Computers," COMPCON 86, IEEE, pp. 254-258 (1986).	
	NPL36	Peleg, A. and Weiser, U., "Future Trends in Microprocessors: Out-of-Order Execution, Speculative Branching and their CISC Performance Potential", IEEE, pp. 263-266 (1991).	
	NPL37	Swensen, J.A. and Patt, Y.N., "Hierarchical Registers for Scientific Computers," Conference Proceedings: 1988 International Conference on Supercomputing, ICS, July 4-8, 1988 (July 4-8, 1988).	
	NPL38	Third-Generation TMS320 User's Guide, Texas Instruments (1988).	
	NPL39	Vin et al., "Instruction Scheduling in High-Performance Architectures - MIDR Algorithm," CIPS Edmonton '88, Chaos Into Order, Proceedings, Edmonton, Alta., Canada, pp. 69-75 (Nov. 7, 1988).	
	NPL40	Wilson, J.E. et al., "On Tuning the Microarchitecture of an HPS Implementation of the VAX," Proceedings of the 20th Annual Workshop on Microprogramming, IEEE Computer Society, pp. 162-167 (December 1-4, 1987).	

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